

**AMENDMENTS TO THE CLAIMS:**

Please replace the claims with the claims provided in the listing below wherein status, amendments, additions and cancellations are indicated.

1. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element having an MFMISS (metal-ferroelectric-metal-insulator-semiconductor) structure formed in a semiconductor substrate, comprising:

an MFM (metal-ferroelectric-metal) structure and an MIS (metal-insulator-semiconductor) structure ~~stacked up and down~~ vertically arranged with the MFM structure above a level of the MIS structure; and

means for increasing [[the]] an effective area of a capacitance of the ~~lower~~ MIS structure as compared with the effective area of a capacitance of the ~~upper~~ MFM structure, the means for increasing the effective area including a lower layer of the MIS structure being formed as one of a trench and a rugged portion such as to increase a surface area thereof of an interface of an insulator layer and a substrate layer of the MIS structure.

2. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element according to claim 1, ~~further having a semiconductor substrate and a~~ wherein the trench is formed in the semiconductor substrate, wherein the MIS

structure is formed in the trench, the MFM structure is laminated on the trench nearly in parallel with the main surface of the semiconductor substrate, and means for increasing the effective area is the trench.

3. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element according to claim 2, wherein the MIS structure is an MIS transistor of the nonvolatile memory element, the regions of source, base and drain of the MIS transistor are formed in the semiconductor substrate in order of source, base and drain from the lower side, and the means for increasing the effective area is a gate structure of the MIS transistor formed on the inner surface of the trench.

4. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element according to claim 2, wherein the MIS structure is an MIS transistor of the nonvolatile memory element, the regions of source, base and drain of the MIS transistor are formed in the semiconductor substrate in order of drain, base and source from the lower side, and the means for increasing the effective area is a gate structure of the MIS transistor formed on the inner surface of the trench.

5. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element according to claim 2, wherein the MIS structure is a MIS

transistor of the nonvolatile memory element, and the regions of source and drain of the MIS transistor are ~~isolated~~ separated by the trench.

6. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element according to claim 1, wherein the MIS structure includes [[a]] the rugged portion therein, the means for increasing the effective area is constituted by the rugged portion, the upper part of the MIS structure is flat, and the MFM structure is laminated thereon.

7. (Currently Amended) A transistor-type ferroelectric nonvolatile memory element according to claim 1, wherein the means for increasing the effective area is constituted by an MIM (metal-insulator-metal) structure provided between the MFM structure and the MIS structure.

8. (Original) A transistor-type ferroelectric nonvolatile memory element according to claims 2 to 7, wherein the effective area of a metal layer on the ferroelectric layer of the MFM structure is smaller than that of the ferroelectric layer.

**AMENDMENTS TO THE DRAWINGS:**

Please find accompanying this response replacement sheets for Figs. 12-16 wherein amendments are effect incorporating the legend "PRIOR ART."